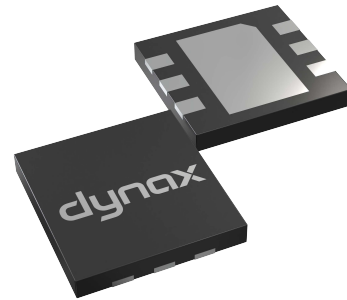


DXG1PH60P-60N

RF Power GaN Transistor



1. Product profile

1.1 General description

DXG1PH60P-60N is a 60 W unmatched RF GaN HEMT Transistor with first generation RF GaN technology from Dynax, which is ideal for cellular base station applications at frequencies from DC to 6 GHz.

Table 1. Typical performance

Freq (MHz)	P_{sat}^1 (dBm)	P_{avg}^2 (dBm)	η_D^2 (%)	G_P^2 (dB)	ACPR ² (dBc)
1805~1880	47.8	40.0	55.0	19.5	-30.0

¹ Test condition: Pulsed CW, Pulse width = 100 μ s, Duty cycle = 10 %.

² Typical Doherty performance in Dynax Demo with the device soldered onto the heatsink, test condition: $V_{DS} = 48$ V, $I_{DQA} = 45$ mA, $V_{GSB} = -5.0$ V, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF. ACPR measured in 3.84 MHz channel bandwidth @ ± 5 MHz offset.

1.2 Features and benefits

- > High efficiency, high gain
- > Microcell base station
- > Designed for Digital Pre-Distortion error correction systems

1.3 Applications

- > RF power amplifier for base stations in the 1805 MHz to 1880 MHz frequency range

1.4 Lead-free and RoHS compliant



5. Thermal characteristics

Table 4. Thermal characteristics

Parameter	Symbol	Value	Unit
Side A, Carrier			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 7.9\text{ W}$	$R_{\text{thjc}}(\text{IR})$	5.4	$^{\circ}\text{C/W}$
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 7.9\text{ W}$	$R_{\text{thjc}}(\text{FEA})$	8.4	$^{\circ}\text{C/W}$
Side B, Peaking			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 7.9\text{ W}$	$R_{\text{thjc}}(\text{IR})$	5.4	$^{\circ}\text{C/W}$
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{\text{base-plate}} = 85^{\circ}\text{C}$, $P_D = 7.9\text{ W}$	$R_{\text{thjc}}(\text{FEA})$	8.4	$^{\circ}\text{C/W}$

6. ESD protection characteristics

Table 5. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2012)	1A (> 250 V)
Charged Device Model (per JESD22-C101F)	C1 (> 250 V)

7. Moisture sensitivity level

Table 6. Moisture sensitivity level

Test methodology	Class
Moisture Sensitivity Level (per J-STD-020)	Level 3

8. Electrical characteristics (TA = 25°C unless otherwise noted)

Table 7. DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Side A, Carrier					
Drain-Source Leakage Current (V _{GS} = -10 V, V _{DS} = 150 V)	I _{DSS}	-	-	3.2	mA
Drain-Source Breakdown Voltage (V _{GS} = -10 V, I _D = 3.2 mA)	V _{(BR)DSS}	150	-	-	V
Gate Threshold Voltage (V _{DS} = 48 V, I _D = 3.2 mA)	V _{GS(th)}	-4.0	-3.2	-1.0	V
Gate Quiescent Voltage (V _{DS} = 48 V, I _D = 80 mA)	V _{GS(Q)}	-	-3.0	-	V
Side B, Peaking					
Drain-Source Leakage Current (V _{GS} = -10 V, V _{DS} = 150 V)	I _{DSS}	-	-	3.2	mA
Drain-Source Breakdown Voltage (V _{GS} = -10 V, I _D = 3.2 mA)	V _{(BR)DSS}	150	-	-	V
Gate Threshold Voltage (V _{DS} = 48 V, I _D = 3.2 mA)	V _{GS(th)}	-4.0	-3.2	-1.0	V
Gate Quiescent Voltage (V _{DS} = 48 V, I _D = 80 mA)	V _{GS(Q)}	-	-3.0	-	V

Table 8. RF characteristics (Typical Doherty performance – 1880 MHz) ¹

Parameter	Symbol	Min.	Typ.	Max.	Unit
Peak Output Power ²	P _{sat}	47.0	48.0	-	dBm
Drain Efficiency ³	η _D	39.0	46.0	-	%
Power Gain ³	G _P	16.6	18.2	19.8	dB

¹ Typical Doherty performance in Dynax DXG1PH60P-60N production test fixture, test condition: V_{DS} = 48 V, I_{DQA} = 60 mA, V_{GSB} = -2.0 V + V_{GSQ} @ 5.0 mA.

² Test condition: Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

³ Test condition: P_{out} = 39.5 dBm Avg., Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF.

Table 9. Load mismatch

Parameter	Result
VSWR 10:1 at V _{DS} = 48 V, 60 W Pulsed CW output power, Pulse width = 100 μs, Duty cycle = 10%.	No device damage

9. Test information

9.1 Graphic Data

9.1.1 Pulsed CW

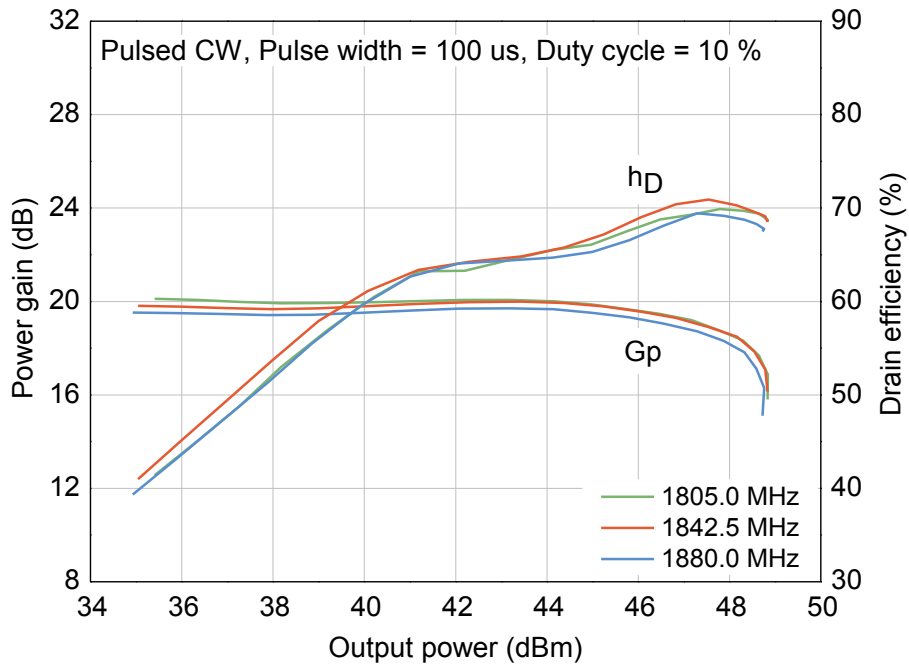


Fig 2. Power gain, Drain efficiency vs. Pulse output power

9.1.2 Single-Carrier W-CDMA

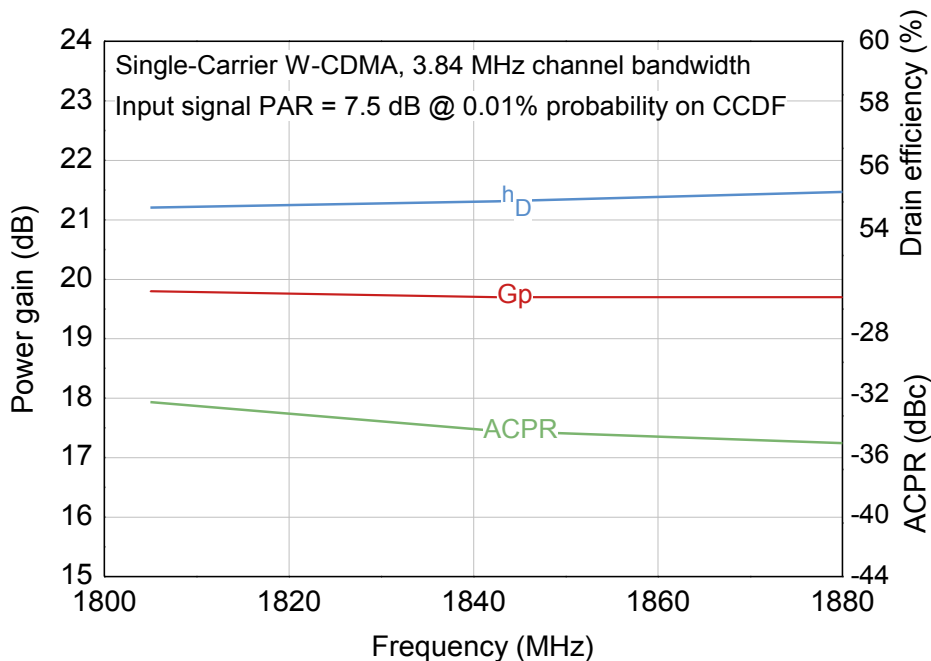


Fig 3. Power gain, Drain efficiency, ACPR vs. Frequency
Single-Carrier W-CDMA @ $P_{out} = 10.0$ Watts Avg.

10. Impedance information

Table 10. Typical impedance of carrier ¹

Maximum Output Power						
Freq (MHz)	Z _S (Ω)	Z _L (Ω)	G _P (dB)	P _{sat} (dBm)	P _{sat} (W)	η _D (%)
1800	3.8 + j3.9	19.7 + j6.8	23.9	46.2	41	68.3
1880	4.1 + j3.8	19.0 + j7.2	23.6	46.2	42	69.7
2110	6.2 + j1.1	20.0 + j5.8	22.4	46.0	40	71.2
2170	6.2 + j1.1	17.0 + j6.3	22.3	45.8	38	71.4
2500	5.5 - j6.3	16.9 + j3.0	21.2	45.9	39	69.6
2700	5.7 - j6.5	13.7 + j3.2	20.7	45.8	38	70.4
Maximum Drain Efficiency						
Freq (MHz)	Z _S (Ω)	Z _L (Ω)	G _P (dB)	P _{sat} (dBm)	P _{sat} (W)	η _D (%)
1800	3.8 + j3.9	12.9 + j22.0	25.7	44.4	27	81.2
1880	4.1 + j3.8	14.5 + j24.0	24.2	44.0	25	80.6
2110	6.2 + j1.1	12.0 + j19.5	23.2	43.9	25	81.7
2170	6.2 + j1.1	12.8 + j20.6	22.4	43.9	25	82.9
2500	5.5 - j6.3	9.8 + j15.3	22.6	43.9	24	82.2
2700	5.7 - j6.5	10.2 + j13.6	21.0	44.1	26	79.5

Table 11. Typical impedance of peaking ²

Maximum Output Power						
Freq (MHz)	Z _S (Ω)	Z _L (Ω)	G _P (dB)	P _{sat} (dBm)	P _{sat} (W)	η _D (%)
1800	3.8 + j3.9	19.7 + j6.8	23.9	46.2	41	68.3
1880	4.1 + j3.8	19.0 + j7.2	23.6	46.2	42	69.7
2110	6.2 + j1.1	20.0 + j5.8	22.4	46.0	40	71.2
2170	6.2 + j1.1	17.0 + j6.3	22.3	45.8	38	71.4
2500	5.5 - j6.3	16.9 + j3.0	21.2	45.9	39	69.6
2700	5.7 - j6.5	13.7 + j3.2	20.7	45.8	38	70.4
Maximum Drain Efficiency						
Freq (MHz)	Z _S (Ω)	Z _L (Ω)	G _P (dB)	P _{sat} (dBm)	P _{sat} (W)	η _D (%)
1800	3.8 + j3.9	12.9 + j22.0	25.7	44.4	27	81.2
1880	4.1 + j3.8	14.5 + j24.0	24.2	44.0	25	80.6
2110	6.2 + j1.1	12.0 + j19.5	23.2	43.9	25	81.7
2170	6.2 + j1.1	12.8 + j20.6	22.4	43.9	25	82.9
2500	5.5 - j6.3	9.8 + j15.3	22.6	43.9	24	82.2
2700	5.7 - j6.5	10.2 + j13.6	21.0	44.1	26	79.5

¹ V_{DS} = 48 V, I_{DQA} = 80 mA, Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

² V_{DS} = 48 V, I_{DQB} = 80 mA, Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

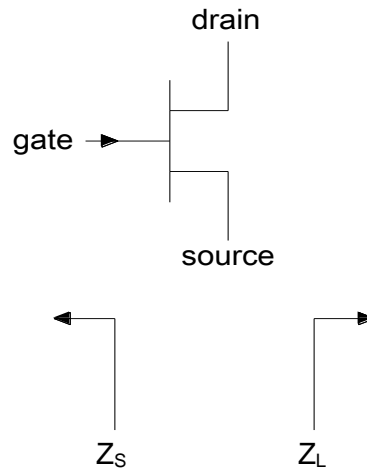


Fig 4. Definition of transistor impedance

11. Median lifetime

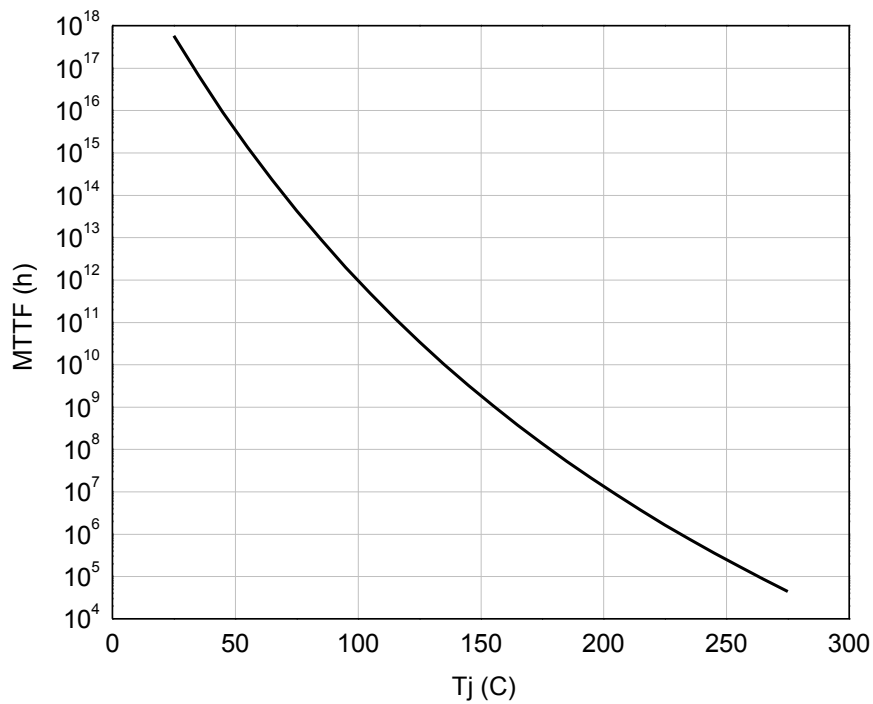
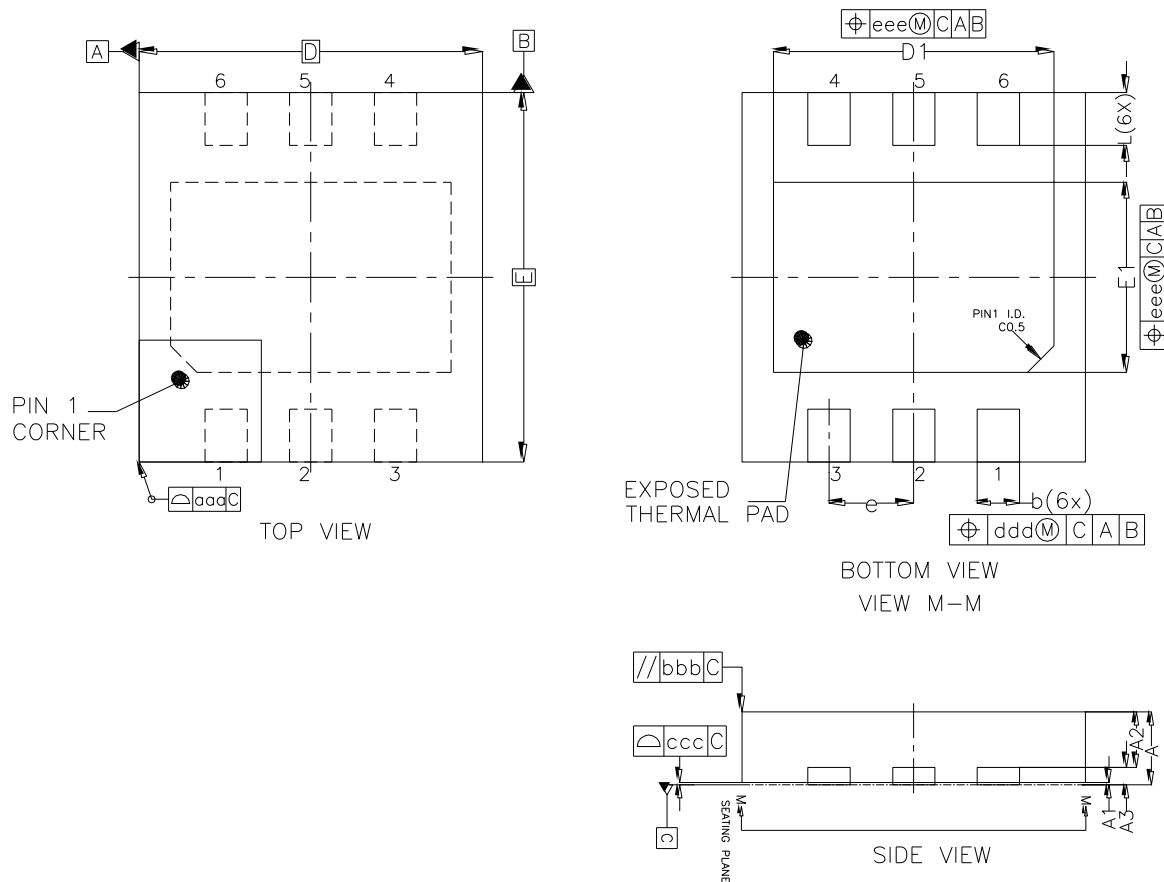


Fig 5. Median lifetime vs. channel temperature

12. Package outline



DESCRIPTION	SYMBOL	MILLIMETER			
		MIN	NOM	MAX	
TOTAL THICKNESS	A	0.80	0.85	0.90	
STAND OFF	A1	0.00	---	0.05	
MOLD THICKNESS	A2	0.60	0.65	0.70	
L/F THICKNESS	A3	0.203 REF			
BODY SIZE	X	D	6.43	6.50	6.57
	Y	E	6.93	7.00	7.07
LEAD PITCH	e	1.60 BSC			
LEAD WIDTH	b	0.75	0.80	0.85	
LEAD LENGTH	L	0.95	1.00	1.05	
EP SIZE	D1	5.26	5.31	5.36	
	E1	3.55	3.60	3.65	
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	bbb	0.1			
LEAD COPLANARITY	ccc	0.08			
LEAD POSITION OFFSET	ddd	0.1			
EXPOSED PAD OFFSET	eee	0.1			

Fig 6. Package outline — DFN 7x6.5mm

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	Electro-Static Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing Wave Ratio

14. Legal information

14.1 Datasheet status

Document status	Product status	Definition
Objective [short] datasheet	Engineering sample	This document contains data from the objective specification for product development.
Preliminary [short] datasheet	Engineering sample	This document contains data from the preliminary specification.
Production [short] datasheet	Mass product	This document contains the product specification.

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